



## **MIMOS R&D SYMPOSIUM**

**2006**

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13 & 14 DECEMBER 2006

SUNWAY LAGOON RESORT HOTEL

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Richard Keating  
Zulfiqar Ali Abdul Aziz

## P R O G R A M

### DAY ONE | 13 December 2006

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- 08.00am – 08.45am : Registration/Breakfast
- 08.45am – 08.50am : Doa Recital by Tuan Haji Ismail Yusof
- 08.50am – 09.00am : Opening remarks by VP of Corporate Human Resource, Puan Hasnah Ismail
- 09.00am – 09.45am : Keynote Address I - “*Getting the Most Out of Your Grid*” by Dr Raj Godhia, Managing Director of Mekarprise Sdn Bhd
- 09.45am – 10.30am : Break and Posters Session

#### SESSION 1

*Moderator: Dr Normaziah Abdul Aziz*

- 10.30am – 11.00am : Paper 1 – Low Yield Troubleshooting of a 0.5um CMOS Product  
Presenter: Wan Sabeng Wan Adini
- 11.00am - 11.30am : Paper 2 – Elimination of Dielectric Etch by Product in MIM Capacitor Fabrication  
Presenter: Ahmad Sabirin Zoolfakar
- 11.30am – 12.00pm : Paper 3 – Contact Etching Process Development for 0.35um Analog Mixed Signal Product  
Presenter: Azlina Mohd Zain
- 12.00pm – 12.30pm : Paper 4 – Analysis on ISFET – Chemical Sensor by using Ag/AgCl Reference Electrode  
Presenter: Rozina Abdul Rani
- 12.30pm – 02.00pm : Lunch
- 02.00pm – 02.15pm : Video Session - *Idea Power*

## P R O G R A M

#### SESSION 2

*Moderator: Mr Foo Lai Ning*

- 02.15pm – 02.45pm : Paper 5- On Iterative Frame Synchronization  
Presenter: Ayman Ahmed
- 02.45pm – 03.15pm : Paper 6 - Learning Old Trick from the Master: Shell Coding at its Finest  
Presenter: Azhar Abu Talib
- 03.15pm – 03.45pm : Paper 7 - Quality of Polarization Entanglement in Spontaneous Parametric Down Conversion  
Presenter: Dr Suhairi Saharudin
- 03.45pm – 04.15pm : Paper 8 - Fine Frequency Offset Estimation for Frequency-Selective Channels  
Presenter: Ayman Ahmed
- 04.15pm – 4.30pm : Break
- 04.30pm – 05.30pm : Unzip Your Mind - " *The Role of Systematic Innovation in Applied Research*" by Mr Joseph Tan, SHRDC

**END OF DAY ONE**

## P R O G R A M

### DAY TWO | 14 December 2006

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- 08.00am – 08.30am : Registration/Breakfast
- 08.30am – 09.15am : Keynote Address II – “*Building World-Class Enterprises with CMMI and People CMM*”  
by Mr Raghav Nandyal, Sitara Technologies

#### SESSION 3

*Moderator: Mr Tan Kong Yew*

- 09.15am – 09.45am : Paper 9 - Water Minimization Using Water Management Network Technique  
Presenter: Nor Razi Misran
- 09.45am – 10.15am : Paper 10 – Guidelines to Create Standard Cell LEF for 0.5um Technology  
Presenter: Norhasniza Othman
- 10.15am – 10.30am : Break

#### SESSION 4

*Moderator: Prof Dr Zaharin Yusof*

- 10.30am – 11.00am : Paper 11 – Performance Analysis of Fully Differential Two-Stage Operational Transconductance Amplifiers Using Different Frequency Compensation Techniques  
Presenter: Yuzman Yusoff
- 11.00am – 11.30am : Paper 12 – A Single-Stage Folded Cascode Gain Boost Amplifier for 10-bit 50-MS/s Pipelined Analog-to-Digital Converter  
Presenter: Tan Kong Yew
- 11.30am – 12.00pm : Paper 13 – Characterizing the Performance on ARM7TDMI-SDRAM in an Embedded System  
Presenter: Mohd Yusri Mohd Yusoff
- 12.00pm – 12.30pm : Paper 14 – A Microcontroller-based Platform for 2-axis low-g Accelerometer in Automotive Application  
Presenter: Mohamad Sofian Abu Talip

## P R O G R A M

- 12.30pm – 02.00pm : Lunch
- 02.00pm – 02.30pm : Video session - *Why didn't I think of that?*

#### SESSION 5

*Moderator: Prof Dr Mohamed Ridza Wahiddin*

- 02.30pm – 03.00pm : Paper 15 – An English-Malay Translation Memory Using Phrase Look-up Approach and Word Alignment Information Database  
Presenter: Suhaimi Ab Rahman
- 03.00pm – 03.30pm : Paper 16 – A Practical Approach in Preparing Data for English-Malay Translation System  
Presenter: Noorhayati Ahmad
- 03.30pm – 04.00pm : Paper 17 – Horizontal Tomcat Clustering to Enhance Speed Performance of MIMOS Online Machine Translation System  
Presenter: Hafizullah Amin Hashim
- 04.00pm – 04.30pm : Refreshment
- 04.30pm – 05.00pm : ‘Fun Learning Quiz’ Prize Giving

## A B S T R A C T

### **Paper 1 – Low Yield Troubleshooting of a 0.5um CMOS Product**

*Authors: Wan Sabeng Wan Adini, Bazura Abd Rahim, Azlina Mohd Zain, Norazah Abd Rashid, Walid Suradi*

Functional electrical test results of a 0.5um CMOS product showed a high percentage of open and short failures that leads to low yield. Failure analysis performed on the failed region through liquid crystal and FIB techniques revealed tungsten residues that remained in bad topography area within the first metal spacing. These tungsten residues had caused shorting of the second metal lines. Several approaches to improve the topography of the first interlayer dielectric (ILD1) had been experimented. We have demonstrated that using thicker SOG film along with optimization of the SOG etchback process had been successful in eliminating the residue, thereby, increasing the product yield.

### **Paper 2 – Elimination of Dielectric Etch by Product in MIM Capacitor Fabrication**

*Authors: Ahmad Sabirin Zoolfakar, Azlina Mohd Zain, Nor Aishah Osman and Bazura Abdul Rahim*

Fabrication of metal-insulator-metal (MIM) capacitor involved dry etching process of the dielectric film which is to be used as the insulator. A by-product of organometallic compound that contained fluorine and metallic elements was found deposited at the sidewall of the MIM capacitor test structure during visual inspection after dielectric etching. The by-product was irremovable by plasma resist strip and solvent cleaning. The dielectric etching process condition was optimized to reduce the formation of the unwanted by-product. It has been proven that the formation of the by-product was successfully prevented by optimizing the etch process parameters and the solvent cleaning time.

### **Paper 3 – Contact Etching Process Development for 0.35um Analog Mixed Signal Product**

*Authors: Azlina Mohd Zain, Ahmad Sabirin Zoolfakar, and Muhamad Ramdzan Buyong*

Polysilicon-insulator-polysilicon (PIP) capacitor and polyresistor sub-modules had been incorporated with a standard 0.35um CMOS technology to produce an Analog Mixed Signal (AMS) product. Addition of the analog sub-modules has created topography height difference between the PIP capacitor region and the MOS transistor region, consequently, varies the thickness of the pre-metal dielectric (PMD) film where contact holes will be formed. Etching contact holes on such topography along with different etch stop materials is challenging. A contact etching process that fulfilled the AMS product

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requirements had been developed through optimization experiments. The findings of the experiments are presented and discussed in this paper.

### **Paper 4 – Analysis on ISFET – Chemical Sensor by using Ag/AgCl Reference Electrode**

*Authors: Rozina Abdul Rani, Othman Sidek, Mohd Ismahadi Syono and Ibrahim Mat*

The behaviour of ion sensitive field effect transistor (ISFET) has been analyzed. ISFET is used as a chemical sensor. ISFET has been fabricated by using MIMOS 1  $\mu\text{m}$  CMOS process technology. During fabrication process, ISFET was deposited with  $\text{Si}_3\text{N}_4$  as ion sensitive material using plasma enhanced chemical vapor deposition (PECVD). The main purpose of doing this analysis is to authenticate the design, fabrication process and functional test of ISFET. These activities have been carried out in-house. In order to define the ISFET characterization, solid type (pellet) and double junction type of Ag/AgCl reference electrode has been used during the analysis. Different types of electrode produce different level of ISFET sensitivity as well as ISFET stability. All the analysis results will be discussed in detail in this paper.

### **Paper 5- On Iterative Frame Synchronization**

*Author: Ayman Ahmed*

Iterative receiver techniques provide a powerful tool to enhance receiver performance and are gradually becoming the norm in modern communication systems. In this paper, we investigate the impact of using iterative frame synchronization in a coded packet communication system in terms of false acquisition probability (FAP), mean squared channel estimation error (MSCEE), un-coded bit error rate (BER) and block error rate (BLER) under additive white Gaussian noise (AWGN) and frequency-selective channels. Our simulations show substantial FAP and MSCEE gains and moderate BER and BLER gains. We also propose a new low-complexity optimized inner iteration technique that offers performance gains close to those achieved by the more demanding outer iterations.

### **Paper 6 - Learning Old Trick from the Master: Shell Coding at its Finest**

*Author: Azhar Abu Talib*

This paper is tribute to among the first shellcode ever written in programming history – if not the first in its own right. It started with a programming contest for bad C codes that started in 1984 called IOCCC, which still continues on until today. In the year that IOCCC first started, Sjoerd Mullender & Robbert van Renesse submitted a piece of code that resembles the shellcodes of today –

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where the executable is written in the data area, which normally are arrays of some type. The Mullender code – as it is called – was among the winners of IOCCC for that year. An analysis of the Mullender is given in this paper with a twist that it prints a "hello world", rather than the original smileys, as a tradition in the programming world. What would the subject of this paper is to completely overhauled the Mullender codes to run on current generation of computers compared to the PDP-11 or VAX-11, where these machines are almost obsolete nowadays.

### **Paper 7 - Quality of Polarization Entanglement in Spontaneous Parametric Down Conversion**

*Authors: Suryadi Soekardjo, Norshamsuri Ali, Dr Suhairi Saharudin and Prof. Dr.*

*Mohamed Ridza Wahiddin*

We experimentally demonstrate a high degree of polarization entanglement known as entanglement visibility through spontaneous parametric down conversion process pumped by a femtosecond laser. The entangled-photon pair was obtained using two type-I BBO crystal. The down-converted photons from these crystals demonstrates a high visibility of 98.7% ( $\theta_2 = 0^\circ$ ) and 90% ( $\theta_2 = 22.5^\circ$ ). These results are in agreement with the theory which expects high visibility from such arrangement.

### **Paper 8 - Fine Frequency Offset Estimation for Frequency-Selective Channels**

*Author: Ayman Ahmed*

In this paper we address the problem of frequency offset estimation from non-periodic training sequences used in packet transmission over frequency-selective channels and additive white Gaussian noise. Based on polynomial approximations of the sin and cos terms in the joint likelihood function, we obtain closed-form expressions of the maximumlikelihood estimate of the frequency offset using standard optimization techniques. We show that, for small frequency offsets, the proposed solutions outperform conventional methods that use large size fast Fourier transforms (FFT). In addition, they can be used with small size FFT's to cover a larger estimation range.

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### **Paper 9 - Water Minimization Using Water Management Network Technique**

*Authors: Mohd Hisham Samingin Co-Author:Nor Razi Misran*

In wafer fabrication industries, huge amount of water is used to produce wafers. A large portion of water is used to produce Deionized Water (DIW). DIW is used to clean wafers that have been processed with hazardous chemical inside the process tools in the cleanroom. Creating DIW is amongst the most expensive and energy intensive steps in the fabricating process of wafers, thus, any decrease in water demand can result in significant savings. For Mimos Semiconductor, to making up city water or fresh water to DIW cost RM9.71 per m<sup>3</sup>. On September 2005, Mimos Semiconductor paid RM 66,466 per month which amount to 128 m<sup>3</sup> of water for each wafer.

### **Paper 10 – Guidelines to Create Standard Cell LEF for 0.5um Technology**

*Authors: Nurafizah Saidin, Wee Leong Son, Norhasniza Othman, and Noor Shelida Salleh*

The paper presents a specific approach to LEF generation. Aimed to provide 0.5um technology abstract information in standard digital design flow. Also, it describes the macro and standard cell information for a design.

### **Paper 11 – Performance Analysis of Fully Differential Two-Stage Operational Transconductance Amplifiers Using Different Frequency Compensation Techniques**

*Authors: Yuzman Yusoff, Rohana Musa and Mohd Rais Ahmad*

Design of two-stage operational transconductance amplifier (OTA) requires some form of frequency compensation in order to ensure stability. This paper analyzes and compares four frequency compensation techniques for fully differential two-stage OTAs. The frequency compensation methods that have been examined using 0.35um TSMC-Like CMOS process are Miller compensation, Ahuja-style compensation, improved Ahuja compensation and hybrid compensation. A fixed topology is employed through out this work; a folded-cascode first stage and a common-source second stage. Their performances on DC gain, unity gain bandwidth, phase margin, settling time and power consumption are extracted from HSPICE simulations. The simulation results are compared and presented in this paper.

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### **Paper 12 – A Single-Stage Folded Cascode Gain Boost Amplifier for 10-bit 50-MS/s Pipelined Analog-to-Digital Converter**

*Authors: Tan Kong Yew , Nabihah Razali, Rohana Musa and Dr. Mohd Rais Ahmad*

An operational transconductance amplifier (OTA) was designed for the sample and hold stage of a 10-bit 50-Mega-Sample-per-second (MS/s) pipelined analog-to-digital converter (ADC). The OTA uses gain boost topology to achieve both high DC gain and high unity gain bandwidth simultaneously. A brief discussion on this topology is covered followed by an analysis of design considerations used during implementation. Simulation results shows DC gain of 95dB, unity gain bandwidth of 412 MHz and 75 degree of phase margin in 0.35um CMOS technology.

### **Paper 13 – Characterizing the Performance on ARM7TDMI-SDRAM in an Embedded System**

*Authors: Mohamad Yusri Mohamad Yusoff and Ahmad Raif Mohamed Noor Beg*

There is more to the performance of an embedded system than the MIPS of the microcontroller alone. This is especially important for microcontroller like the ARM7TDMI that lacks cache memories. The performance of the memory devices used will have a direct impact to the overall performance. While the characterization of the microcontroller performance running on memory devices like Flash and SRAM is straightforward, the characterization on SDRAM is rather complicated. This paper uses the result of running a program on the ModelSim simulator to come up with a performance characterization of code running on ARM7TDMI on SDRAM.

### **Paper 14 – A Microcontroller-based Platform for 2-axis low-g Accelerometer in Automotive Application**

*Authors: Mohamad Sofian Abu Talip, Ibrahim Mat, Mohd Arif Safaruddin Mohd Najmi, Mohd Ismahadi Syono & Rozina Abd Rani*

The design and implementation of a microcontroller-based platform for 2-axis low-g accelerometer in an automotive application is presented. The first device is designed to collect the data out from the 2-axis low-g accelerometer sensor, relay them to the host computer via the serial port and store them on the computer memory. A graphical user interface (GUI) has been developed using LabView for fully output visualization. The second design is focusing on portability and low power consumption for battery-driven applications. Both of the design focuses are to detect the vibration and inclination of unit under test (UUT) for further usage in an automotive application. A PIC microcontroller is used as the central control unit for the data flow coordination. The system

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prototype can be readily miniaturized using surface mount technology (SMT) or hybrid techniques.

### **Paper 15 – An English-Malay Translation Memory Using Phrase Look-up Approach and Word Alignment Information Database**

*Authors: Suhaimi Ab Rahman Normaziah Abdul Aziz*

This paper describes the searching method employed in a Translation Memory (TM) for translating English to Malay language. It applies sentence level and phrase look-up matching techniques. In sentence level matching, the system generates the translations of the input sentences by searching for the exact matched sentence from the TM. As for phrase look-up matching, the system locates the translation fragments in several examples. The system then generates the translation suggestion by combining these translation fragments. Both techniques generate a translation suggestion with the assistance of word alignment information. With such a system, any newly translated sentence together with its translation, can be learned and added into the translation memory. In this way, the translation memory grows dynamically during the translation process. As the number of entries grows, the translation memory is able to produce better results of translation suggestions to its user, particularly the translator.

### **Paper 16 – A Practical Approach in Preparing Data for English-Malay Translation System**

*Author: Noorhayati Ahmad*

Preparing data is an important preprocessing step in creating parallel corpus for the translation system. This is because of the input data will strongly influence the translation result. The good quality input data will produce good translation result and vice-versa. This paper describes on how data is being prepared with various technical/computing tools. It also explains the importance of the involvement of translator and linguist at the very beginning of the data preparation. The author will also share the experiences and challenges when working with cross-disciplinary team members.

### **Paper 17 – Horizontal Tomcat Clustering to Enhance Speed Performance of MIMOS Online Machine Translation System**

*Authors: Hafizullah Amin Hashim, Wan Mohd Hikam Kauthary Hassan*

Machine Translation (MT) is a sub-field of computational linguistics that investigates the use of computer software to translate text or speech in between natural languages. In this initiative, MIMOS Knowledge Technology Lab has come out with Online Machine Translation to provide a better translation service for the users. However, currently it happens that the speed

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of the web based machine translation getting slow due to intensive concurrent user access. To solve this problem, MIMOS Knowledge Technology Lab has invited MIMOS Grid Computing Lab to work together to grab the fastest solution. Therefore, in this paper we shall highlight the method used by the team to improve the velocity and thus enhance the overall performance which is required within a limited time frame. An upgraded version of Horizontal Tomcat clustering is used to undertake this concern. Consequently, a comparison between the translation speed on the single and clustered web-servers (counted in word per second) will be provided to show that clustered system is able to speed up the translation process.



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Chairman, MS2006

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Vice Chairman, MS2006

*Dr Normaziah Abdul Aziz*

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*Prof Dr Zaharin Yusof*

*Prof Dr Mohamed Ridza Wahiddin*

Panel Judges

*Prof Dr Mazlan Abbas*

*Prof Dr Masuri Othman*

*Dr Hon Hock Woon*

*Dr Mabrouk*

*Dr Wan Latifah Wan Mohamad*

Emcee

*Ahmad Sabirin Zoolfakar*

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and

to all who have in one way or another contributed to the success of  
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